ADLINK
LEADING EDGE COMPUTING

Express-TL

COM Express Basic Size Type 6 Module with 11th Gen Intel® Core™, Intel® Xeon® and Celeron® Processors

Preliminary

Features

- Intel® Tiger Lake-H Processors, up to 8 cores, integrated Intel® UHD Graphics (Xe architecture)
- AI inference (AVX512 VNNI + Intel® UHD GFX)
- Up to 128GB DDR4 SO-DIMM, non-ECC and ECC
- 3x DDI channels, 1x LVDS (opt. 4 lanes eDP), opt. VGA, up to 4 independent displays, 8K capable
- PCIe x16 Gen4, 2.5GbE (TSN, build option)
- Extreme Rugged operating temperature: -40°C to +85°C (build option, selected SKUs)

Specifications

• Core System

CPU

11th Gen Intel Xeon, Core and Celeron Processors (Tiger Lake-H)

Xeon® W-11865MRE 2.6(4.2)GHz, 45(35W cTDP) (8C/32EU)

Core™ i7-11850HE 2.6(4.2)GHz, 45W(35W cTDP) (8C/32EU)

Xeon® W-11555MRE 2.6(4.1)GHz, 45(35W cTDP) (6C/32EU)

Core™ i5-11500HE 2.6(4.1)GHz, 45W(35W cTDP) (6C/32EU)

Xeon® W-11155MRE 2.4(4.0)GHz, 45(35W cTDP) (4C/16EU)

Core™ i3-11100HE 2.4(4.0)GHz, 45W(35W cTPD) (4C/16EU)

Celeron® 6600HE 2.6GHz, 35W (2C/16EU)

Supports: Intel® VT, Intel® VT-d, Intel® TXT, Intel® SSE4.2, Intel® HT Technology, Intel® 64 Architecture, Execute Disable Bit, Intel® Turbo Boost Technology 2.0, Intel® AVX-512, Intel® AVX2, Intel® AES-NI VT, Intel® VT-d, Intel® TXT, Intel® SSE4.2, Intel® HT Technology, Intel® 64 Architecture, Execute Disable Bit, Intel® Turbo Boost Technology 2.0, Intel® AVX-512, Intel® AVX2, Intel® AES-NI, PCLMULQDQ Instruction, Intel® Secure Key and Intel® TSX-NI.

Notes:

Availability of features may vary between processor SKUs.

Additional low TDP SKUs are not listed, please check manual.

Some SKUs listed above are supported by project basis only. Please contact your ADLINK epresentative for availability.

Memory

Dual channel up to 3200 MT/s DDR4 memory up to 128GB in four SODIMM sockets

Two SO-DIMM on top side, two SO-DIMM on bottom side (3 or 4 socket versions by build option)

ECC support by Xeon CPU paired with RM590E PCH

Embedded BIOS

AMI UEFI with CMOS backup in 32 or 16MB (TBC) SPI BIOS (dual BIOS by build option)

Cache

24MB for W-11865MRE, i7-11850HE / 12MB for W-11555MRE, i5-11500HE / 8MB for W-11155MRE, i3-11100HE, Celeron 6600HE

Chipset

RM590E (support ECC, with Xeon CPU)

QM580E

HM570E

Expansion Busses

PCIe x16 Gen4 (CD): Lanes 15-31 (configurable to one x16, two x8, one x8 + two x4)

6 PCIe x1 Gen3 (AB): Lanes 0/1/2/3 (configurable to x1, x2, x4) and Lanes 4/5 (x2, x1)

2 PCIe x1 Gen3 (CD): Lanes 6/7 (configurable to x2, x1)

LPC bus (through an ESPI to LPC bridge IC), SMBus (system) , I²C (user)

SEMA Board Controller

Supports: Voltage/current monitoring, power sequence debug support, AT/ATX mode control, logistics and forensic information, flat panel control, general purpose I2C, watchdog timer, fan control and failsafe BIOS (dual BIOS by build option)

Debug Headers

30-pin multipurpose flat cable connector for use with DB-30 x86 debug module providing BIOS POST code LED, EC access, SPI BIOS flashing, power testpoints, debug LEDs

• Video

GPU Feature Support

Intel® Gen 12 Graphics Core Architecture, Supporting multiple independent and simultaneous display combinations of DisplayPort/HDMI/LVDS, eDP or VGA outputs (4x 4K60) (8K60 at eDP and DDI 1/2 will occupy two display pipelines and requires much more memory capacity)

Hardware encode/transcode of HD content (including HEVC)

DirectX 12 support

OpenGL 4.5, 4.4/4.3 and ES 2.0 support

OpenCL 2.1, 2.0/1.2 support

Digital Display Interface

DDI1/2/3 supporting DisplayPort/HDMI/DVI

VGA

Supported by build option through DP-to-VGA IC (in place of DDI3), max. resolution 1920x1200@60Hz

LVDS

Single/dual channel 18/24-bit LVDS from eDP-to-LVDS IC, max. resolution 1920x1200@60Hz in dual mode

eDP

Build option: 4 lane support, in place of LVDS, max. resolution 8K@60Hz (TBC, may require re-timer on carrier and is memory bandwidth dependent)

Note: "build option" indicates an alternative BOM configuration to support additional or alternative functions that are not available on the standard product. Be aware that these "build option" part numbers will need to be newly created and this will result in production lead times.

Specifications

Audio

Chipset

Intel® HD Audio integrated on CPU

Audio Codec

On carrier Express-BASE6 (ALC886 standard support)

Ethernet

Intel® MAC/PHY

LAN controller i225 series (i225-IT feature TSN by build option)

Interface

2.5GbE and 1000/100/10 Mbit/s Ethernet connection

GbE0_SDP available if TSN support enabled

I/O Interfaces

USB: 4x USB 3.2/2.0/1.1 (USB 0,1,2,3) and 4x USB 2.0/1.1 (USB 4,5,6,7)

SATA: 4x SATA 6Gb/s (SATA 0,1,2,3)

On-board Storage: Soldered type PCIe based SSD (build option)

Serial: 2x UART ports with console redirection

GPIO/SD: 4x GPO and 4x GPI from EC (GPI with interrupt TBC)

Note: USB 3.1 Gen2 support dependent on carrier design

Super I/O

Supported on carrier if needed (standard support for W83627DHG-P, other Super I/O supported by project basis)

TPM

Chipset: Infineon

Type: TPM 2.0 (SPI based)

Power

Standard Input: ATX: 12V±5% / 5Vsb ±5%; or AT: 12V±5%

Wide Input: ATX: 8.5-20 V / 5Vsb ±5%; or AT: 8.5-20V

Management: ACPI 5.0 compliant, Smart Battery support

Power States: C1-C6, S0, S1, S3, S4, S5 , S5 ECO mode (Wake on USB S3/S4, WOL S3/S4/S5)

ECO mode: supports deep S5 mode for power saving

Mechanical and Environmental

Form Factor: PICMG COM.0: Rev 3.0 Type 6

Dimension: Basic size: 125 mm x 95 mm

Operating Temperature

Standard: 0°C to 60°C (storage: -20°C to 80°C)

Extreme Rugged: -45°C to +85°C (storage: -40°C to 85°C, build option, selected SKUs, TBC)

Humidity

5-90% RH operating, non-condensing

5-95% RH storage (and operating with conformal coating)

Shock and Vibration

IEC 60068-2-64 and IEC-60068-2-27

MIL-STD-202F, Method 213B, Table 213-I, Condition A and Method 214A, Table 214-I, Condition D

HALT

Thermal Stress, Vibration Stress, Thermal Shock and Combined Test

Operating Systems

Standard Support

Windows 10 IOT Enterprise 64-bit, Yocto project based Linux 64-bit, VxWorks 64-bit (TBC)

Extended Support (BSP)

Yocto project based Linux 64-bit

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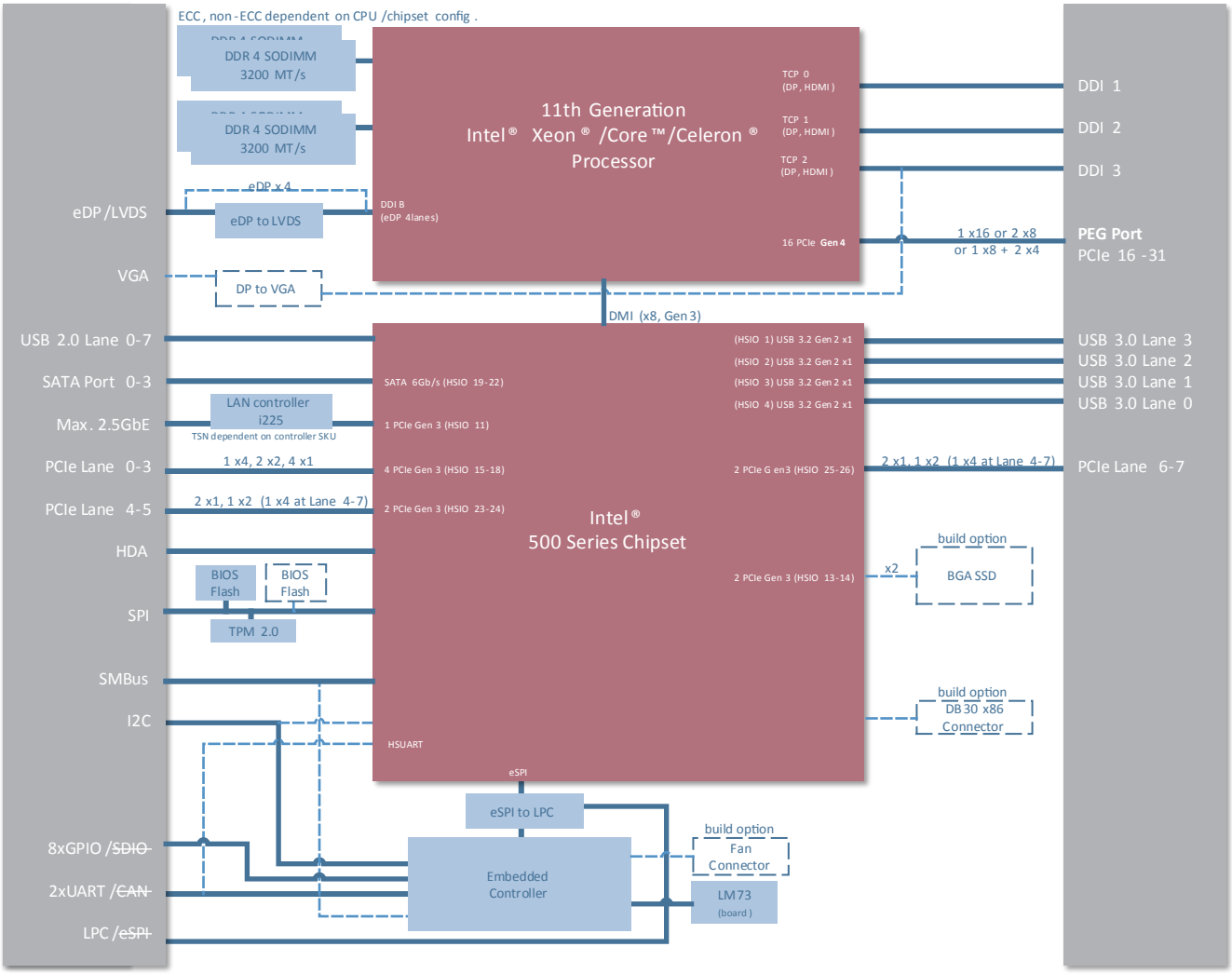
Functional Diagram



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